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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/684,224 | 10/10/2003 | Chen-Hua Yu | TSM03-0403 | 8634 |

43859 7590 01/24/2006

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| EXAMINER |
|---|
| WILLIAMS, ALEXANDER O |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| | | | |
|---|---|---|---|
| ***Office Action Summary*** | **Application No.**<br>10/684,224 | **Applicant(s)**<br>YU ET AL. | AW |
| | **Examiner**<br>Alexander O. Williams | **Art Unit**<br>2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,7-15,17-31 and 57-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,7-15,17-31 and 76-80* is/are allowed.

6)☒ Claim(s) *57-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/684224 Attorney's Docket #: TSM03-0403
Filing Date: 10/10/2003;

Applicant: Yu et al.

Examiner: Alexander Williams

Applicant's Amendment filed 11/10/04 to the election of Group I (original claims 1 to 31), filed 7/12/05, has been acknowledged.

Claims 4, 5, 16 and 32 to 56 have been cancelled.

Claims 71 to 75 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 71 it unclear and confusing to what is meant by "The semiconductor device of claim 71." Applicant has this claim 71 depending on itself 71.

Any of claims 71 to 75 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection **based on a barrier layer and a high temperature superconductor (HTS) layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.**

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 57-63 and 67-75, **insofar as some of them can be understood**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin (U.S. Patent # 6,518,648 B1).

57. Lopatin (figures 1 to 3) specifically figure 3 show a semiconductor device comprising: a dielectric layer **210,212** defining at least one aperture **204** therein; a barrier layer **232 (see column 5, lines 5, lines 30-35)** formed along the bottom and side walls of said at least one aperture; a high temperature superconductor (HTS) layer **232 (see column 5, lines 5, lines 30-35)** formed over and coating the barrier layer in said at least one aperture; and a conductive material **234,236** in direct contact with said HTS layer and filling said aperture in said dielectric layer to form said connecting metalization.
58. The semiconductor device of claim 57, Lopatin show wherein the dielectric layer is a low-k dielectric material.
59. The semiconductor device of claim 57, Lopatin show wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations of these materials.
60. The semiconductor device of claim 57, Lopatin show wherein the HTS material is a rare earth cuprate (copper oxide) material.
61. The semiconductor device of claim 57, Lopatin show wherein the HTS material is a rare earth element combined with barium copper oxide.
62. The semiconductor device of claim 61, Lopatin show wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holnuum and lutetium.
63. The semiconductor device of claim 61, Lopatin show wherein the FITS material is yttrium barium copper oxide.
67. The semiconductor device of claim 57, Lopatin show wherein the HTS layer has a thickness of between 10A to 500A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
68. The semiconductor device of claim 57, Lopatin show wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.
69. The semiconductor device of claim 57, Lopatin show wherein the aperture defined in said dielectric has a width less than about 300.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

70. The semiconductor device of claim 57, Lopatin show wherein said at least one aperture includes at least two trenches.
71. The semiconductor device of claim 71, Lopatin further comprising a capping layer over said conductive metal filling said at least one aperture.
72. The semiconductor device of claim 71, Lopatin show wherein said capping layer is an HTS capping layer.
73. The semiconductor device of claim 71, Lopatin further comprising another dielectric layer over said first dielectric layer and said HTS capping layer.
74. The semiconductor device of claim 74, Lopatin further including a hard mask over said HTS capping layer.
74. The semiconductor device of claim 74, Lopatin said hark mask is a layer of ARC.

Therefore, it would have been obvious to one of ordinary skill in the art to use the barrier layer and the HTS layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

S-PAT-NO: 6518648

DOCUMENT-IDENTIFIER: US 6518648 B1
**See image for Certificate of Correction**

TITLE: Superconductor barrier layer for integrated circuit interconnects

DATE-ISSUED: February 11, 2003

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
| Lopatin; Sergey D. | Santa Clara | CA | N/A | N/A |

ASSIGNEE INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY | TYPE CODE |
|---|---|---|---|---|---|
| Advanced Micro Devices, Inc. | Sunnyvale | CA | N/A | N/A | 02 |

APPL-NO: 09/ 671944

DATE FILED: September 27, 2000

ABSTRACT:

An integrated circuit and manufacturing method therefor is provided having a semiconductor substrate with a semiconductor device. A dielectric layer is on the semiconductor substrate and has an opening provided therein. A high temperature superconductor material barrier layer lines the opening and a seed layer is deposited to line the superconductor material barrier layer. A seed layer and a conductor core fills the opening over the barrier layer to form a conductor channel. The superconductor material barrier layer can be of yttrium barium copper oxide deposited by a process, such as laser ablation (LA), chemical vapor deposition (CVD), atomic layer deposition (ALD), or self-ionized plasma (SIP) deposition on a low dielectric constant dielectric layer and having a copper seed layer deposited thereon by SIP deposition.

(11) The barrier layers 226 and 232 are of high temperature oxide superconductor materials such as yttrium barium copper oxide. The materials are multi-layered ceramics and are considered "high temperature" because at temperatures of 77.degree.-92.degree. Kelvin they are superconductive.

(12) The low dielectric constant dielectric layers 208, 212, and 210 are of materials such as TEOS (tetraethoxysilane), TMOS (tetramethoxysilane), OMCTS (octamethyleclotetrasiloxane), and DADBS (diaceloxyditerliarybutoxsilane). These materials are carried in a solvent fluid carrier such as MIBK (methyl isobutyl ketone). One of the more commonly used silicon-based, low dielectric constant materials is HSQ (hydrogen silsesquioxane) in MIBK solvent. A low dielectric constant material has a dielectric constant below 2.8 and is used to reduce capacitance effects which slow the operation of integrated circuits. Other low dielectric constant materials can be used.

(13) The seed layers 228 and 234 and conductor cores 230 and 236 are of materials such as copper, copper-base alloys, gold, gold-base alloys, silver, silver-base alloys, and a combination thereof.

(14) The method for manufacturing an integrated circuit having superconductor material barrier layers includes depositing the dielectric layer 208 over the semiconductor substrate by spin deposition.

(15) After processing the dielectric layer 208 to harden it, a photolithographic process is used to form an opening in the dielectric layer 208. An ammonia (NH.sub.3) plasma treatment is used to treat the low dielectric constant dielectric material in preparation for the deposition of the superconductor material barrier layer 226 to line the opening.

(16) The superconductor material barrier layer 226 is deposited as a conformal barrier-liner by such processes as laser ablation (LA), chemical vapor deposition (CVD), atomic layer deposition (ALD), or self-ionized plasma (SIP) deposition. In the best mode for sub-0.18 .mu.m geometry copper interconnects, the superconductor material barrier layer 226 is deposited to a thickness of from 50 .ANG. to 300 .ANG..

Claims 64 to 66 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lopatin (U.S. Patent # 6,518,648 B1) in view of Hartner et al. (U.S. Patent # 6,649,483 B2).

Lopatin show the features of the claimed invention as detailed above, but fail to explicitly show wherein the HTS material is a rare earth Ruthenium Oxocuprate.

Hartner et al. is cited for showing FeRam memory device. Specifically, Hartner et al. (figures 1 to 3D) specifically figure 2 show a semiconductor device comprising: a first dielectric layer **30** defining at least one aperture therein; a conductive material filling **(within 10)** said at least one aperture in said first dielectric layer; an HTS capping layer **(within 10)** over said conductive material filling said at least one aperture; and another dielectric layer **40** over said first dielectric layer and said HTS capping layer for the purpose of preventing oxidation below the surface of the substrate.

64. The semiconductor device of claim 57, Hartner et al. show wherein said HTS layer is a rare earth Ruthenium Oxocuprate.
65. The semiconductor device of claim 64, Hartner et al. show wherein said rare earth Ruthenium Oxocuprate is defined by the formula RuSr, (rare earth element) CuyOZ in which x is between about 1.55 and 2.45, y is between about 1.55 and 2.45, and z is between about 7.55 and 8.45.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

66. The semiconductor device of claim 64, Hartner et al. show wherein said rare earth element is selected from yttrium.

Therefore, it would be obvious to one of prdinary skill in the art to use Hartner et al.'s HTS layer to modify Lopatin's HTS layer for the purpose of preventing oxidation below the surface of the substrate.

US-PAT-NO: 6649483

DOCUMENT-IDENTIFIER: US 6649483 B2

TITLE: Method for fabricating a capacitor
configuration

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:
NAME CITY STATE
ZIP CODE COUNTRY
Hartner; Walter Glen Allen VA
N/A N/A
Weinrich; Volker Paris N/A
N/A FR
Kronke; Matthias Dresden N/A
N/A DE

ASSIGNEE INFORMATION:
NAME CITY STATE ZIP
CODE COUNTRY TYPE CODE
Infineon Technologies Munich N/A N/A
DE 03
AG

APPL-NO: 09/ 996959

DATE FILED: November 20, 2001

**1.** (36) In order to fabricate ferroelectric capacitors for applications in nonvolatile semiconductor memories having a high integration density, a ferroelectric material, for example SrBi.sub.2 (Ta,Nb).sub.2 O.sub.9 (SBT, SBTN), Pb(Zr,Ti)O.sub.3

(PZT), Bi.sub.4 Ti.sub.3 O.sub.12 (BTO), (Ba,Sr)TiO.sub.3 (BST) or the like, is used as a dielectric between the electrodes of a capacitor. **Paraelectric materials, such as, for example,**
2. **(Ba,Sr)TiO.sub.3 (BST), can also be used. The electrode material is a noble metal which withstands high temperatures in oxygen. Appropriate materials for this are Pt, Pd, Ir, Rh, Ru, RuO.sub.x, IrO.sub.x, RhO.sub.x, SrRuO.sub.3, LSCO (LaSrCoO.sub.x), YBa.sub.2 Cu.sub.3 O.sub.7** and high-temperature superconductors. In general, the capacitor construction involves, in a conventional manner, either following the technologically more demanding stacked principle or else proceeding according to the offset cell principle, which takes up a great deal more space.

Claims 1-3, 7-15, 17-31 and 76-80 are allowed.

## Response

Applicant's arguments filed 11/10/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "1, 25 and new claims 57-80" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∍ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∍ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∍ 1.136(a) WILL BE CALCULATED FROM THE

MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at it time.

| Field of Search | Date |
|---|---|
| U.S. Class and subclass:<br>257/700,701,758,759,760,764,762,766,298,664,663,665, 751 | 8/8/05<br>1/10/06 |
| Other Documentation:<br>foreign patents and literature in<br>257/700,701,758,759,760,764,762,766,298,664,663,665, 751 | 8/8/05<br>1/10/06 |
| Electronic data base(s):<br>U.S. Patents EAST | 8/8/05<br>1/10/06 |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/11/06